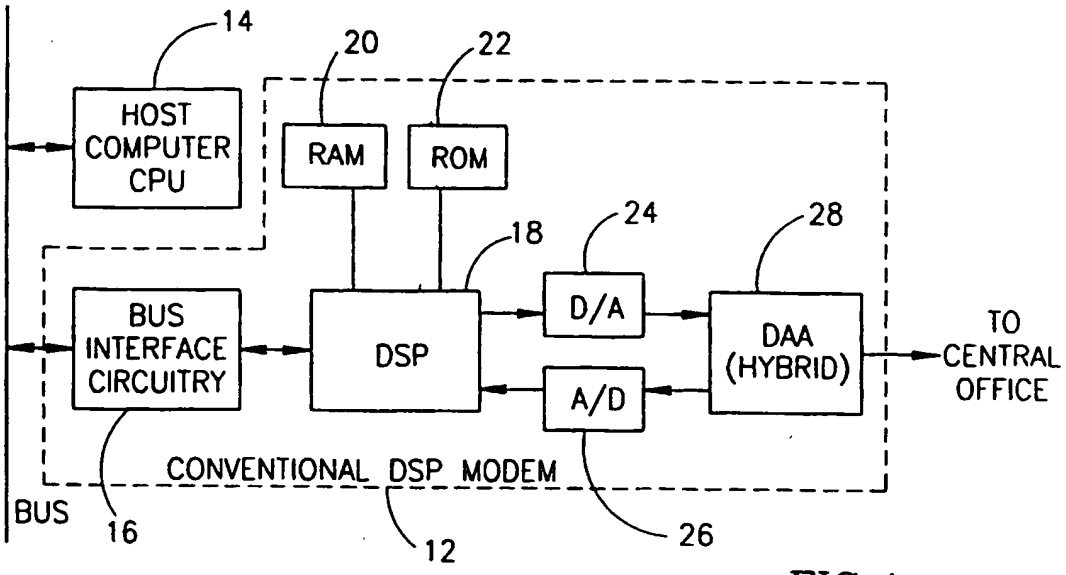


FIG. 1
PRIOR ART

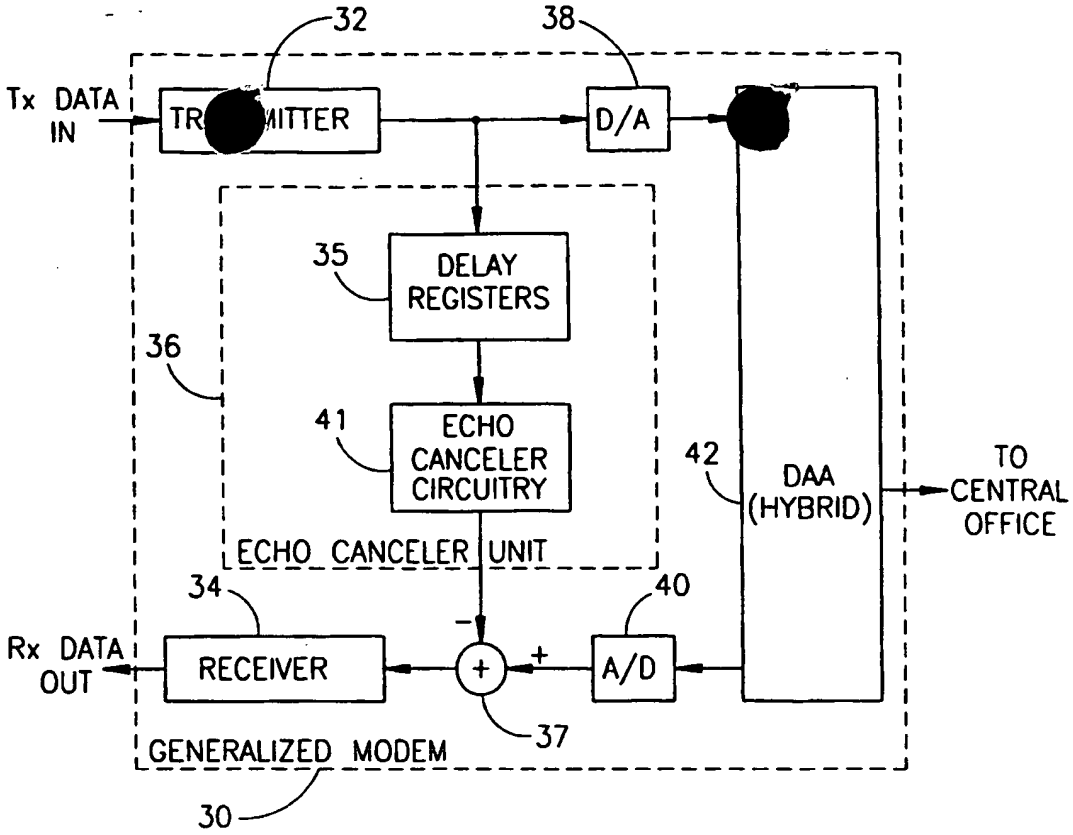
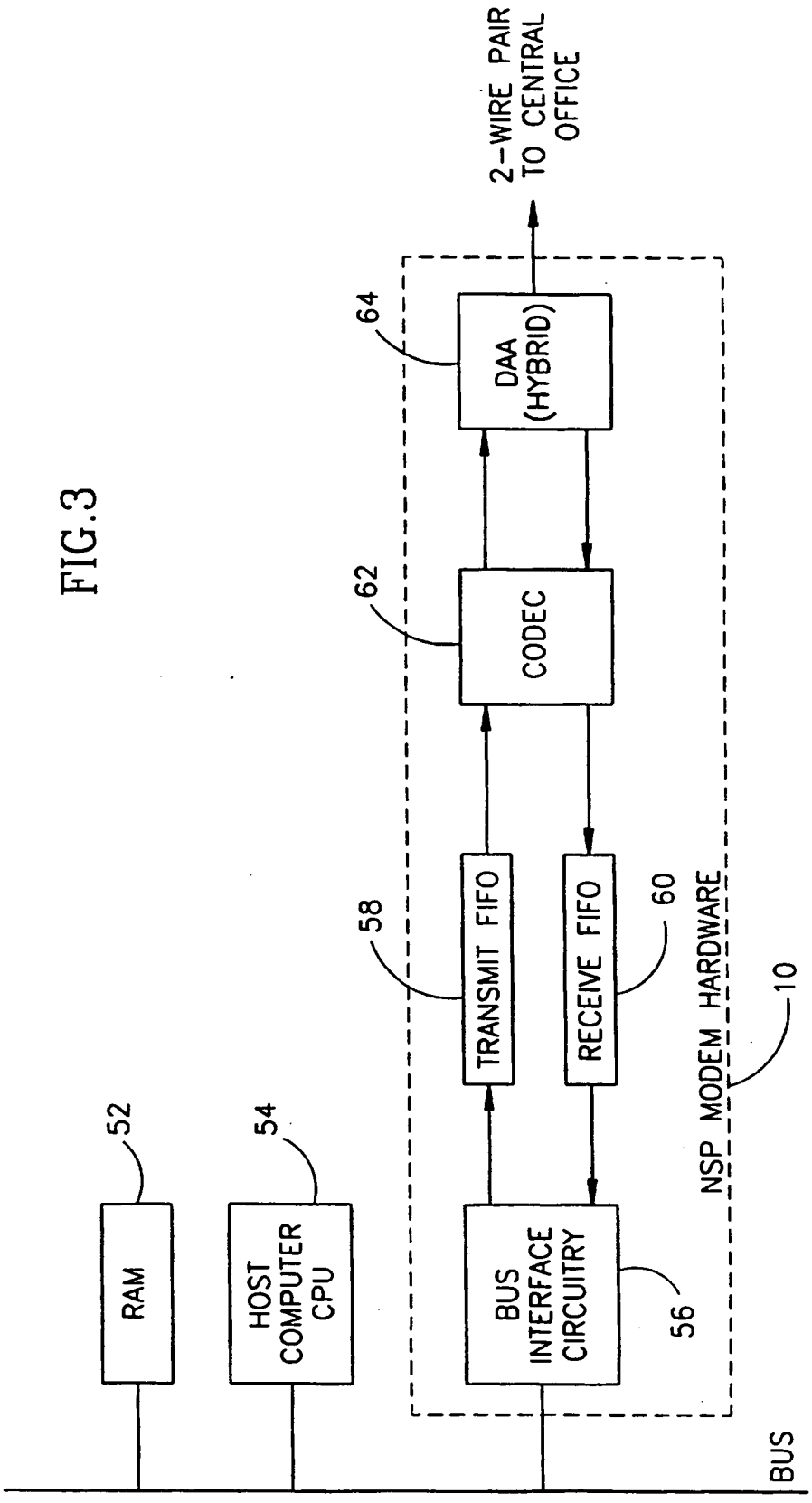

32
38
Tx DATA IN
TRANSMITTER
D/A
35
DELAY REGISTERS
36
41
ECHO CANCELER CIRCUITRY
42
DAA (HYBRID)
TO CENTRAL OFFICE
ECHO CANCELER UNIT
34
40
Rx DATA OUT
RECEIVER
A/D
37
GENERALIZED MODEM
30

FIG.2

FIG.3


2-WIRE PAIR TO CENTRAL OFFICE
64
DAA (HYBRID)
62
CODEC
58
TRANSMIT FIFO
60
RECEIVE FIFO
NSP MODEM HARDWARE
10
52
RAM
54
HOST COMPUTER CPU
BUS INTERFACE CIRCUITRY
56
BUS

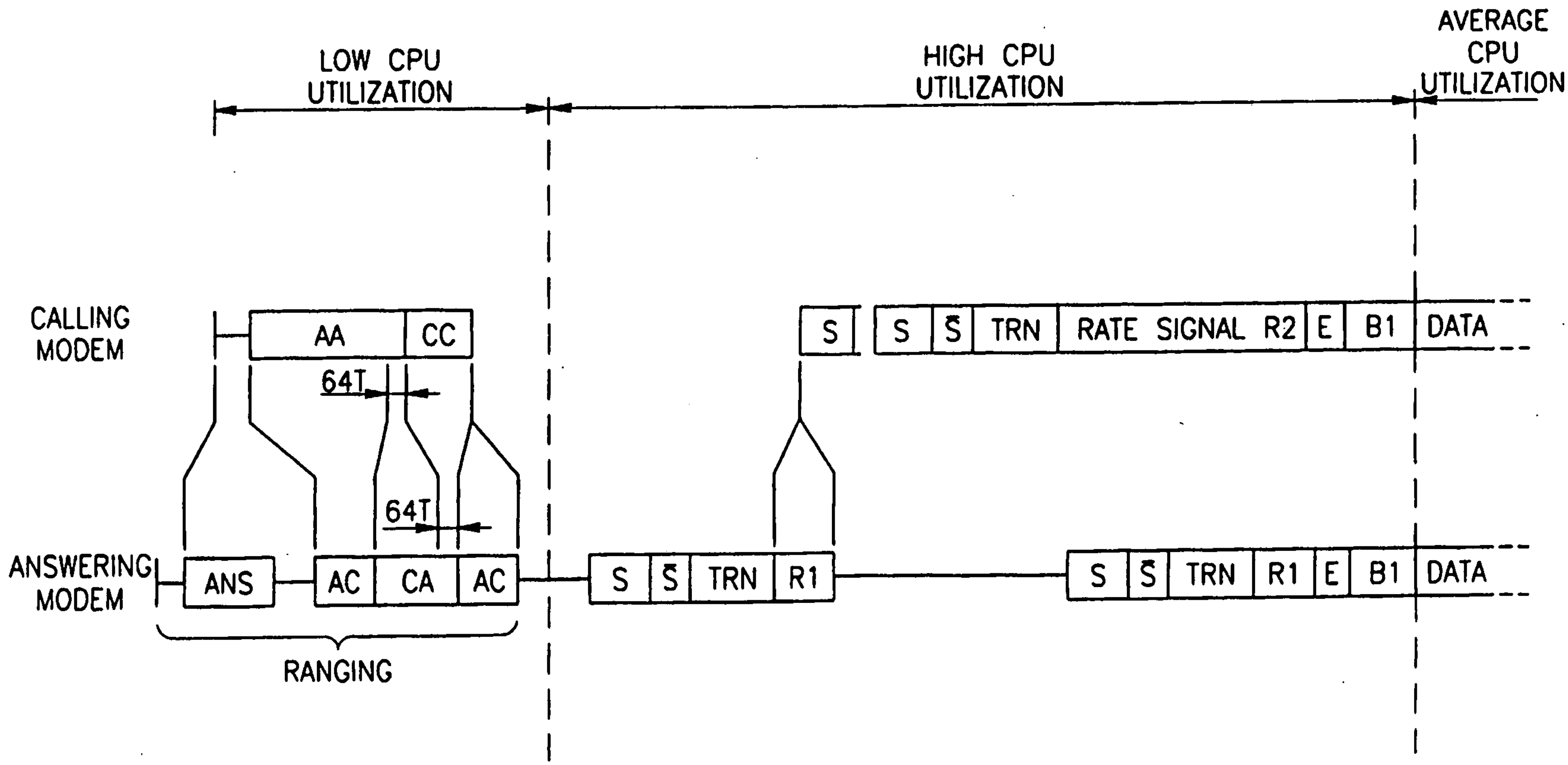

LOW CPU UTILIZATION
HIGH CPU UTILIZATION
AVERAGE CPU UTILIZATION
CALLING MODEM
ANSWERING MODEM
AA
CC
64T
64T
ANS
AC
CA
AC
RANGING
S
S
S̄
TRN
RATE SIGNAL
R2
E
B1
DATA
S
S̄
TRN
R1
S
S̄
TRN
R1
E
B1
DATA

FIG.4

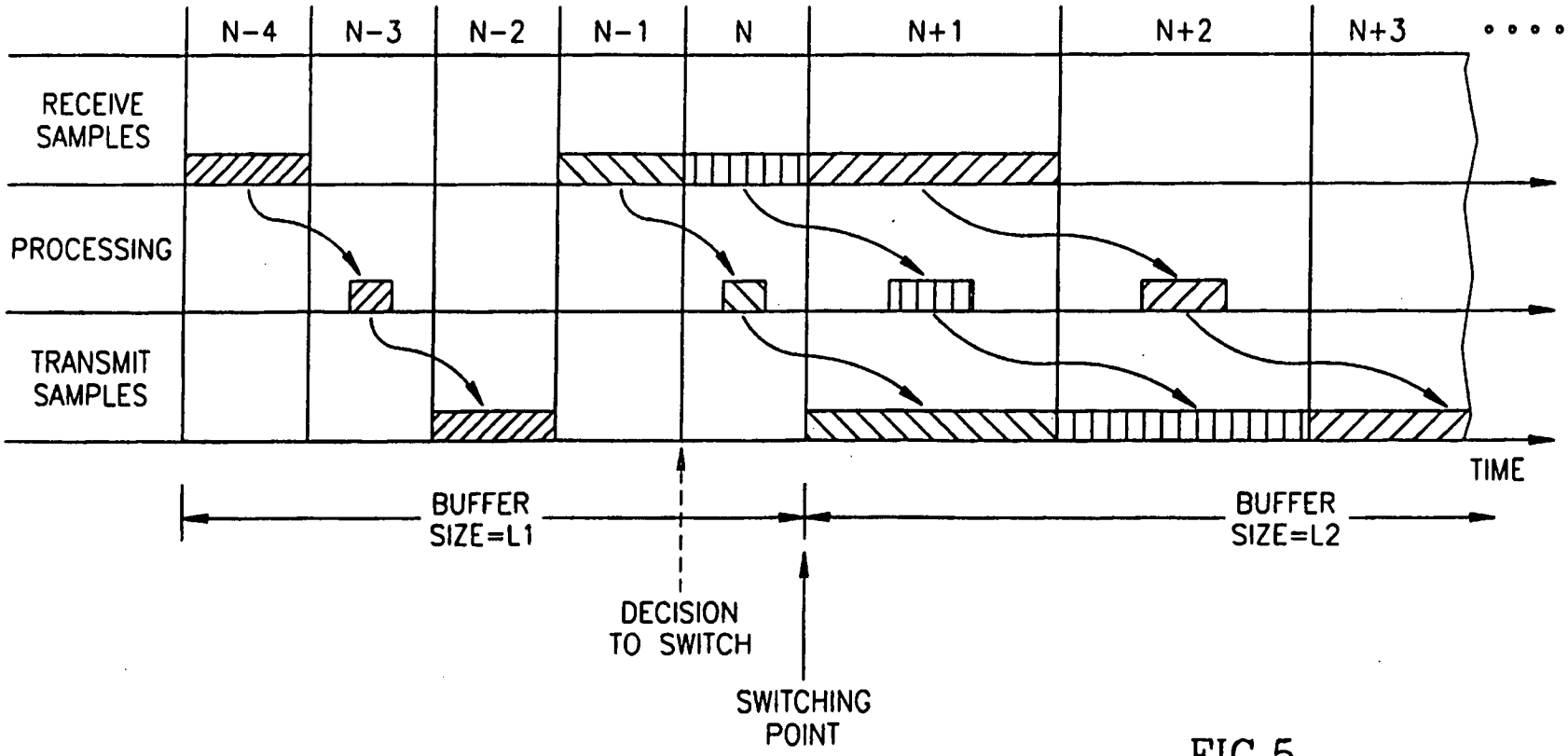


FIG.5

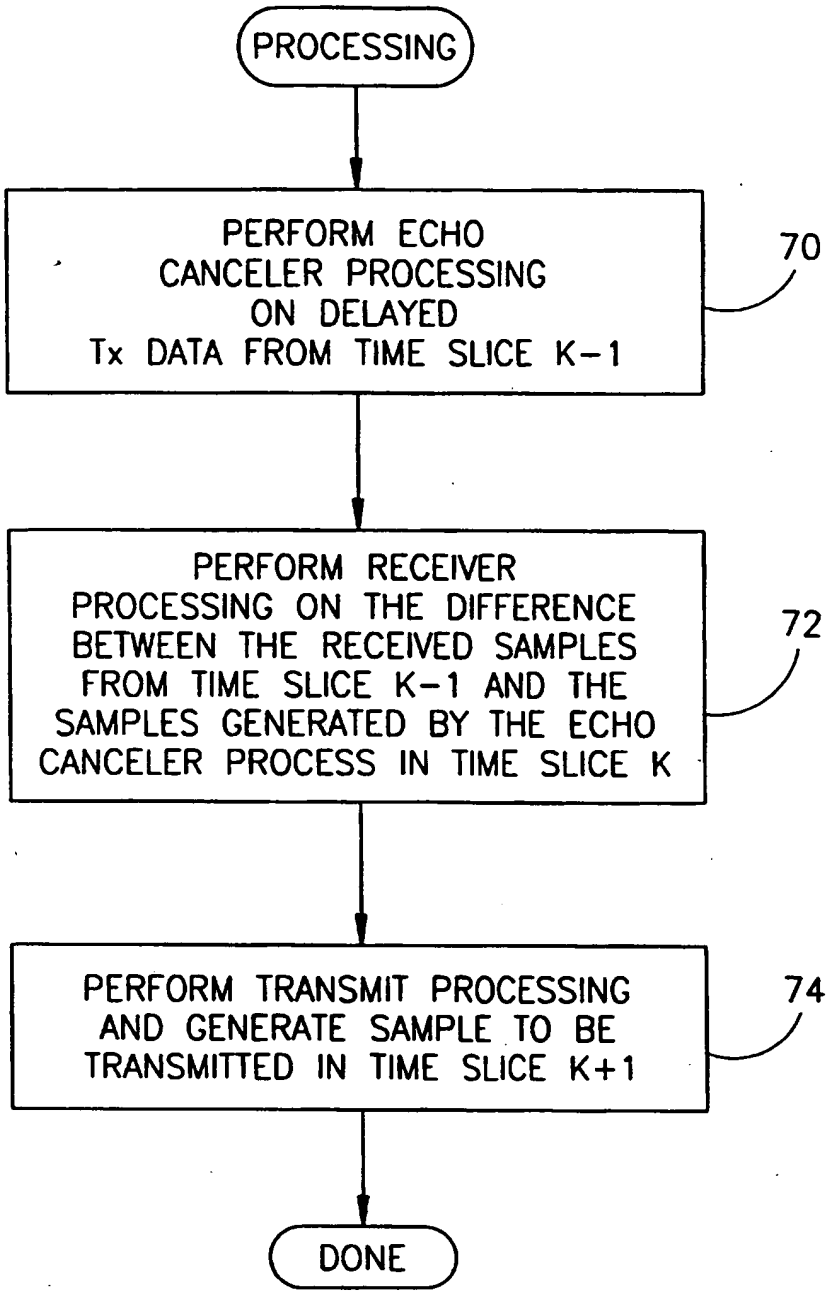

PROCESSING
PERFORM ECHO CANCELER PROCESSING ON DELAYED Tx DATA FROM TIME SLICE K−1
70
PERFORM RECEIVER PROCESSING ON THE DIFFERENCE BETWEEN THE RECEIVED SAMPLES FROM TIME SLICE K−1 AND THE SAMPLES GENERATED BY THE ECHO CANCELER PROCESS IN TIME SLICE K
72
PERFORM TRANSMIT PROCESSING AND GENERATE SAMPLE TO BE TRANSMITTED IN TIME SLICE K+1
74
DONE

FIG.6